CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a power control circuit; and

a plurality of circuit blocks, wherein each of said plurality of circuit blocks has a plurality of states including at least a first state and a second state, further wherein each of said plurality of circuit blocks works in accordance with its function in said first state and rests in said second state, further wherein said power control circuit determines the operation of each of said plurality of circuit blocks so as not to exceed a maximum power consumption of said semiconductor integrated circuit device.

2. The semiconductor integrated circuit device of Claim 1, wherein said power control circuit determines the state of at least one of said plurality of circuit blocks according to the power consumption in said first state and the power consumption required in a transition to said first state.

3. The semiconductor integrated circuit device of Claim 1, further comprising:

a main circuit whose power is not controlled by said power control circuit, wherein said power control circuit, upon receiving a request for accessing one of said plurality of circuit blocks from said main circuit and determining to enable said access to said one circuit block, outputs an enable signal to said main circuit, further wherein said one circuit block makes a transition to said first state.

4. The semiconductor integrated circuit device of Claim 1, wherein said plurality of circuit blocks further comprise:

a first circuit block; and

a second circuit block privileged to access said first circuit block, wherein said power control circuit, upon receiving a request for accessing said first circuit block from said second circuit block and determining to enable said access to said first circuit block, outputs an enable signal to the second circuit, so that said second circuit block makes a transition to said first state.

5. The semiconductor integrated circuit device of Claim 1, wherein said power control circuit and said plurality of circuit blocks are housed in a single package.

6. The semiconductor integrated circuit device of Claim 1, wherein said power control circuit and said plurality of circuit blocks are integrated on a single semiconductor substrate.

7. The semiconductor integrated circuit device of Claim 1, wherein at least one of said plurality of circuit blocks further comprises:

a leakage current control circuit for controlling power consumption by a leakage current; and

a charging/discharging power control circuit for controlling power consumption by charging/discharging of a load, wherein power consumption of said at least one circuit block is controlled in accordance with the state of said at least one circuit block by said leakage current control circuit and said charging/discharging power control circuit.

8. The semiconductor integrated circuit device of Claim 7, further comprising:

a clock distribution system, wherein said charging/discharging power control circuit of said at least one circuit block controls power consumption by charging/discharging of a load, by controlling the clock frequency distributed to said at least one circuit block.

9. The semiconductor integrated circuit device of Claim 1, further comprising:

a non-volatile memory, wherein said maximum power consumption is stored in said non-volatile memory.

10. The semiconductor integrated circuit device of Claim 1, wherein each of said plurality of circuit blocks is configured by a MOS transistor whose threshold voltage is 0.2V or less.

11. The semiconductor integrated circuit device of Claim 1, wherein each of said plurality of circuit blocks is configured by a MOS transistor whose gate oxide thickness is 4nm or less.

12. The semiconductor integrated circuit device of Claim 1, further comprising:

a state transition limiting circuit for limiting the state transition frequency of at least one of said plurality of circuit blocks under a predetermined value.

13. A semiconductor integrated circuit device, comprising:

a first circuit block having a plurality of states with different power consumption values;

a second circuit block privileged to access said first circuit block; and

a power control circuit, wherein said second circuit block is adapted to issue a request for accessing said first circuit block to said power control circuit, further wherein said power control circuit is adapted to determine whether to enable said access to said first circuit block according to a predetermined maximum power consumption, and further wherein said second circuit block is adapted to access said first circuit block when said power control circuit enables said access to said first circuit block.

14. The semiconductor integrated circuit device of Claim 13, wherein said first circuit block comprises:

a leakage current control circuit for controlling power consumption by a leakage current; and

a charging/discharging power control circuit for controlling power consumption by charging/discharging of a load, wherein said plurality of states of said first circuit block include a state in which either power consumption by said leakage current or power consumption by charging/discharging of said load in said first circuit block is limited.

15. The semiconductor integrated circuit device of Claim 13, wherein said power control circuit, when enabling said access to said first circuit block, outputs a signal for enabling said access to said first circuit block to said second circuit block.

16. The semiconductor integrated circuit device of Claim 13, wherein said power control circuit determines whether to enable said access to said first circuit block according to the power consumption required for said first

circuit block to work in accordance with its function and the power consumption required for said first circuit block to make a transition to a state for enabling an access from said second circuit block.